International Symposium on Networks-on-Chip

Call for Papers

15th IEEE/ACM International Symposium on Networks-on-Chip

October 14-15, 2021, Virtual Conference

(*Co-located with Embedded Systems Week 2021*)

https://nocs2021.github.io/

The International Symposium on Networks-on-Chip (NOCS) is the premier event dedicated to interdisciplinary research on on-chip, package-scale, chip-to-chip, and datacenter rack-scale communication technology, architecture, design methods, applications and systems. NOCS brings together scientists and engineers working on NoC innovations and applications from inter-related research communities, including discrete optimization and algorithms, computer architecture, networking, circuits and systems, packaging, embedded systems, and design automation.

(New in 2021) Journal Special Issue: A selected number of accepted papers will be invited to be published in the ACM Journal on Emerging Technologies in Computing Systems, Special Issue on Next-generation On-Chip and Off-Chip Communication Architectures for Edge, Cloud and HPC.

Paper submission website: https://www.softconf.com/l/nocs2021/

More details at https://nocs2021.github.io/

Topics of interest include, but are not limited to:

NoC Architecture and Implementation
- Network architecture (topology, routing, arbitration)
- Timing, synchronous/asynchronous communication
- NoC reliability issues and solutions
- Security issues and solutions in NoC architectures
- Power/thermal issues at NoC un-core and system-level
- Network interface issues and solutions
- Signaling and circuit design for NoC links and routers

Communication Analysis, Optimization, & Verification
- NoC performance analysis and Quality of Service
- Modeling, simulation, and synthesis of NoC
- Verification, debug and test of NoC
- NoC design and simulation methodologies and tools
- Benchmarks, experiences on NoC-based hardware
- Communication-efficient algorithms
- Communication workload characterization & evaluation

Novel NoC Technologies
- Optical, wireless, CNT, and other emerging technologies
- NoC for 2.5D and 3D packages
- Package-specific NoC design
- Network coding and compression solutions
- Approximate computing for NoC and NoC-based systems

NoC for Intelligent Physical Systems
- NoC design for Deep Learning
- Mapping of existing and emerging applications onto NoC
- NoC case studies, application-specific NoC design
- NoC for FPGA, structured ASIC, CMP and MPSoC
- NoC designs for heterogeneous systems
- NoC for CPU-GPU and data-center-on-a-chip (DCoC)
- Scalable modeling of NoC
- Machine learning for NoC and NoC-based Systems

NoC at the Un-Core and System-level
- Design of memory subsystem (un-core) including memory controllers, caches, cache coherence protocols in NoC
- NoC for new memory/storage technologies
- NoC support for processing-in-memory
- OS support for NoC
- Programming models for NoCs
- Interactions between large-scale systems (datacenter, edge and fog computing) and NoC-based building blocks

Inter/Intra-Chip and Rack-Scale Network
- Unified inter/intra-chip networks
- Hybrid chip-scale and datacenter rack-scale networks
- All aspects of inter-chip and rack-scale network design

Organization Committee

General Chairs
Tushar Krishna (Georgia Tech)
John Kim (KAIST)

Technical Program Chairs
Sergi Abadal (Universitat Politècnica de Catalunya)
Joshua San Miguel (University of Wisconsin)

Steering Committee Chair
Radu Marculescu (University of Texas, Austin)

Publicity Chairs
José Luis Abellán (Catholic University of Murcia)
Kun-Chih Chen (National Sun Yat-Sen University)
Jieming Yin (Lehigh University)

Web Chair
Salvatore Monteleone (Kore University of Enna)

Publication Chair
Mahdi Nikdast (Colorado State University)

Industry Chair
Hao Luan (Futurewei Technologies)

Important Dates

Abstract Registration: ~~May 14th~~ … June 11th
Full-paper Submission: ~~May 21st~~ … June 11th

Notification of Acceptance: July 23rd